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A Novel Approach for modelling the Threshold Voltage and Sub threshold Swing of Nano Cylindrical MOSFET

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Abstract

The cylindrical gate-all-around MOSFET has become one of the most promising device structures in the technology scaling roadmap. By completely surrounding the channel, excellent gate control is achieved to reduce short-channel effects. In this paper a novel technique for solving the Poisson equation in cylindrical coordinates for nano cylindrical MOSFET has been developed using the general series solution method. Based on this model, a new compact model for subthreshold swing is formulated. Using the developed model, the variation of threshold voltage, Drain Induced Barrier Lowering (DIBL) and subthreshold swing sensitivities to channel length and channel thickness have been observed. The model is believed to provide a better physical insight and understanding of nano cylindrical MOSFET devices operating in the subthreshold regime. The developed model is verified extensively with MATLAB simulations. The major advantages of the developed model are that, no iterations and no adjustable fitting parameters are required.

Keywords — Nano Cylindrical MOSFET, Poisson equation, Quantum Mechanical Effect (QME), Threshold voltage, Drain current.

I. Introduction

The gate-all-around (GAA) MOSFET is considered one of the most promising devices for downscaling below 50 nm [Auth and Plummer, 1997; Iñíguez et al, 2005; Park and Colinge, 2002; Wann et al, 1996]. Among all the GAA MOSFETS like double gate MOSFET, trigate MOSFET square GAA MOSFET etc, the cylindrical gate-all-around MOSFET has become one of the most promising device structures in the technology scaling roadmap. By completely surrounding the channel by the gate, excellent gate control is achieved to reduce short-channel effects. With the development of MOS devices into deep submicron regime, the scaling theory requires higher substrate doping concentration and thinner gate oxide thickness layer [Baccarani et al., 1984]. This leads to a high transverse electric field at the oxide/semiconductor interface [Liu et al, 2008; Ray and Mahapatra, 2008]. Such a strong field at the interface gives rise to the splitting of the conduction band into discrete subbands and quantum–mechanical effects (QMEs) becomes significant [Ando, Fowler and Stern, 1982; Stern, 1972].

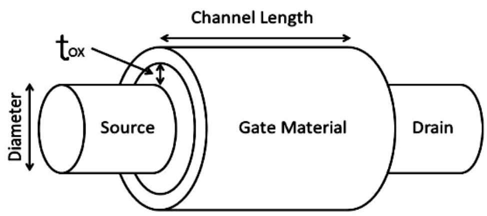

Figure 1. Cylindrical Gate all around MOSFET

2.0 Adopted approaches

2.1 Threshold voltage model

The threshold voltage in case of the Cylindrical surrounding gate-all-around MOSFET can be obtained by solving the one dimensional Poisson's equation. Here, the general series solution method has been used for solving the equation. The one dimensional Poisson's equation for a MOS structure in cylindrical co-ordinate is given by [Sharma, 2009]

$$\frac{1}{r}\frac{\partial}{\partial r}\left[r\frac{\partial}{\partial r}\emptyset(r)\right] = -\frac{\rho}{\varepsilon_{si}} \quad (1)$$

Where

$\emptyset(r)$ - potential distribution in the cylindrical silicon pillar

r - radial direction of the cylindrical coordinate (metre)

ε_{Si} - dielectric permittivity of silicon.

($\varepsilon_{Si}=\varepsilon_{0}\varepsilon_{r}$ =103.59*10^{-12} F/m) ρ - charge density (per metre^3)

By using the general series solution method [Deka, 2012] we obtain

$$\emptyset = a_1 \sum_{m=0}^{\infty} \frac{A^m}{3^2 * 5^2 * 7^2 * \ldots * (2m+1)^2} r^{2m+1} \tag{2}$$

The electric field at the oxide semiconductor interface at the onset of threshold [Singh J., 1997] is given by

$$E_S \Big|_{\emptyset = 2\emptyset_F, r = \frac{t_{si}}{2}} = -a_1 \sum_{m=0}^{\infty} \frac{A^m (2m+1)}{3^2 * 5^2 * 7^2 * \ldots * (2m+1)^2} \left(\frac{t_{si}}{2}\right)^{2m} \tag{3}$$

Bulk charge density [Sharma , 2009] is given by

$$Q_B = -\mathcal{E}_{SiO_2} * E_S = 3.9 * a_1 \sum_{m=0}^{\infty} \frac{A^m (2m+1)}{3^2 * 5^2 * 7^2 * \ldots * (2m+1)^2} \left(\frac{t_{si}}{2}\right)^{2m} \tag{4}$$

Cylindrical oxide capacitance per unit area is [Sharma , 2009]

$$C_{ox-cyl} = \frac{2\mathcal{E}_{ox}}{t_{si} * \ln\left(1 + 2\frac{t_{ox}}{t_{si}}\right)} \tag{5}$$

Threshold voltage is given by [Sharma, 2009]

$$V_{th} = V_{FB} + 2|\emptyset_F| + \frac{|Q_B|}{C_{ox-cyl}} \tag{6}$$

where V_{FB} – Flatband voltage

$\emptyset_F$ - Bulk Fermi potential

$$\emptyset_F = \left(\frac{kT}{q}\right)\ln\left(\frac{N_a}{n_i}\right)$$

2.2 *Threshold voltage model including QME*

To estimate the quantum mechanical V_{th}-shift with a 2-D confinement in a cylindrical structure, it is required to solve the Schrödinger equation and Poissons equation self consistently. Here a parabolic potential well approximation in the cylindrical geometry has been assumed.

As per this assumption, the potential is given as follows:

$$V(r) = F\frac{t_{si}}{2}\left[1 - \left\{\frac{r}{\frac{t_{si}}{2}}\right\}^2\right], \quad r \le t_{si}/2 \tag{7}$$

$$V(r) = \infty, \quad r > t_{si}/2 \tag{8}$$

Where $F = qE_S$

The Schrödinger equation in cylindrical coordinate with a parabolic potential well can be presented as

$$-\frac{\hbar^2}{2m^*}\nabla^2\Psi + F\frac{t_{si}}{2}\left[1 - \left\{\frac{r}{\frac{t_{si}}{2}}\right\}^2\right]\Psi = E\Psi \tag{9}$$

The effective increase in threshold voltage due to QME can be expressed as [Deka, 2012]

$$\Delta V_{th\,qm} = \frac{E_1}{q} \tag{10}$$

Where E_1 - electric field at lowest sub band [Deka, 2012]

Hence the new threshold voltage is given by

$$V_{th\,qm} = V_{th} + \Delta V_{th\,qm}$$

$$= V_{th} + \frac{E_1}{q} \tag{11}$$

2.3 Drain current model

For a cylindrical device neglecting the effect of drain bias, the effective channel width 'W_{eff}' can be found by dividing the current path area by thickness of the current path [Sharma , 2009]

$$W_{eff} = \frac{A}{t_{inv}} = \frac{\pi[t_{si}^2 - (t_{si} - 2t_{inv})^2]}{4t_{inv}}$$

Hence the drain current for a cylindrical gate all around MOSFET is [Streetman and Banerjee, 2001]

For active region (when $V_{GS} - V_{th} > V_{DS}$)

$$I_D = \mu C_{ox\_cyl} \frac{W}{L} [(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}] \tag{12}$$

For saturation region (when $V_{GS} - V_{th} \leq V_{DS}$)

$$I_D = \mu C_{ox\_cyl} \frac{W}{2} (V_{GS} - V_{th})^2 \tag{13}$$

When quantum mechanical effects (QME) is taken into account, the drain current equation for a cylindrical gate all around MOSFET becomes

For active region

$$I_D = \mu C_{ox\_cyl} \frac{W_{eff}}{L} [(V_{GS} - V_{th\,qm})V_{DS} - \frac{V_{DS}^2}{2}] \tag{14}$$

For saturation region

$$I_D = \mu C_{ox\_cyl} \frac{W_{eff}}{2L} (V_{GS} - V_{th\,qm})^2 \tag{15}$$

2.4 Sub threshold swing model

The Subthreshold swing S is defined as the change in the gate bias required to change the subthreshold drain current by one decade and is given by [Godoy et al., 2001]

$$S = \frac{\partial V_{GS}}{\partial \log I_D} \tag{16}$$

where V_{GS} = Gate to source voltage

I_D = Drain Current

In the weak inversion regime there is a potential barrier between the source and the channel region. As the drain voltage is increased, the depletion region of the p-n junction between the drain and body increases in size and extends under the gate. Thus the drain assumes a greater portion of the burden of balancing depletion region charge, leaving a smaller burden for the gate. As a result, the charge present on the gate retains charge balance by attracting more carriers into the channel thus lowering the threshold voltage of the device. This effect is known as drain induced barrier lowering (DIBL) and is given by

$$DIBL = \frac{V_{th}^{DD} - V_{th}^{low}}{V_{DD} - V_{D}^{low}}$$

where

V_{th}^{DD} = threshold voltage measured at a supply voltage

V_{th}^{low} = threshold voltage measured at a very low drain voltage

V_{DD} = supply voltage

V_{D}^{low} = low drain voltage

3. Results and Discussions

Figure 2. shows the dependence of threshold voltage (with and without including QME) on doping concentration for Aluminium gate for different values of silicon film thickness. When QME is taken into account, the conduction band edge goes up. As a result of this, the gate voltage required is little more to bring the conduction band below the Fermi level by the same amount thus increasing the threshold voltage. For higher value of silicon film thickness, threshold voltage increases sharply.

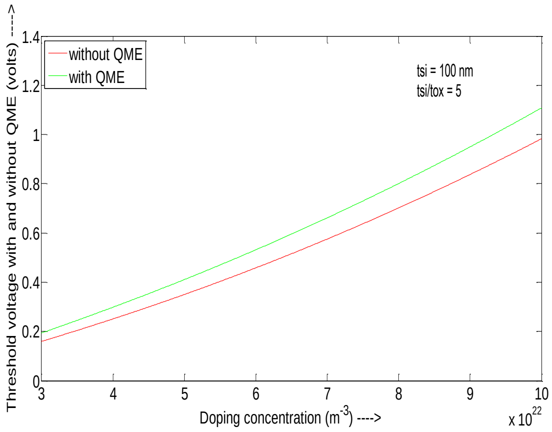

Figure 2. Threshold voltage (with and without including QME) vs. Doping concentration for Aluminium gate for silicon pillar thickness (tsi) of 100 nm

Figure 3. shows the dependence of threshold voltage including QME on silicon pillar diameter for Aluminium gate and n^+ polysilicon gate. It is observed that when the silicon pillar diameter increases the threshold voltage decreases steeply and then attains a constant value.

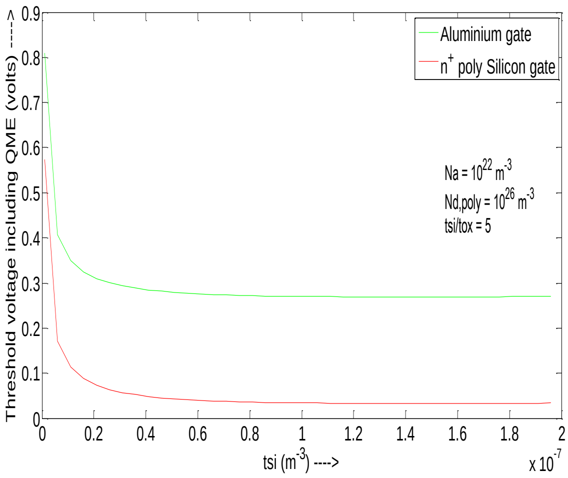

Figure 3. Threshold voltage including QME vs. silicon pillar diameter for Aluminium gate and n^+ polysilicon gate

Figure 4. shows the variation of drain current considering QME with channel length for various values of silicon film thickness in case of Aluminium gate. Drain current increases as the channel length is decreased.

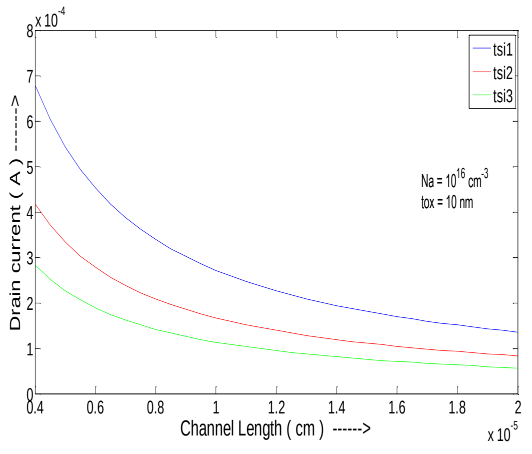

Figure 4. Drain current considering QME vs. Channel length for various values of silicon film thickness (tsi1 = 100 nm, tsi2 = 60 nm and tsi3 = 40 nm) for Aluminium gate.

Figure 5. shows the variation of Subthreshold Swing as a function of channel length for Vds = 0.1 V. DIBL increases as the channel length is decreased. Figure 6. shows the variation of DIBL as a function of channel length for tsi = 50 nm and tox = 10 nm. DIBL increases as the channel length is decreased

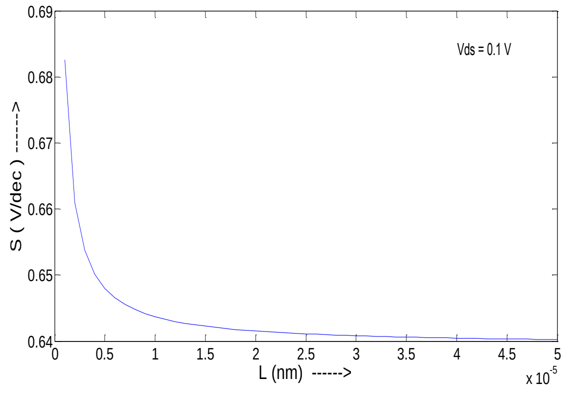

Figure 5. Subthreshold Swing as a function of Channel length with tox = 10 nm and tsi = 50 nm.

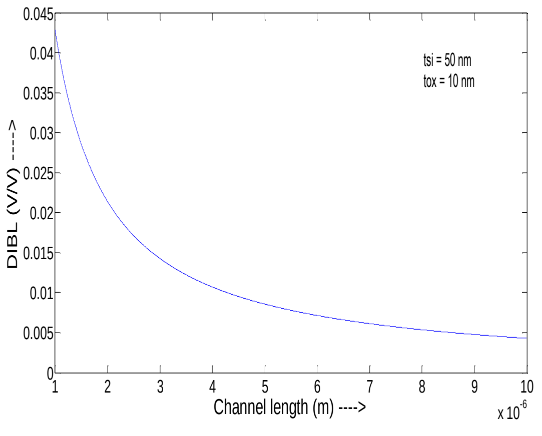

Figure 6. DIBL plotted as a function of Channel length

4. Conclusion

As the MOSFET devices are scaled down to deep sub-micron dimensions, ultra thin oxide thickness and higher levels of channel doping are required for minimizing undesirable short channel effects which causes significant bending of the energy bands at the interface. This makes the potential well adequately narrow. Thus the classical movement of the charge carriers is greatly affected by the non-classical behaviour of the electrons in the narrow potential well. The modelling approach for estimation of quantum mechanical energy band shift uses parabolic potential well (PPW) approximation, for decoupling the Schrodinger and Poisson's equation. Using the developed model, the effect of variation on threshold voltage, gate current, drain current; with the extension into the saturation regime along with the variation of substrate doping, silicon pillar diameter, drain to source voltage and gate to source voltage are observed. Since our model is formulated for moderate doping concentration, hence a large discrepancy from the classical analysis is seen in the device characteristics while obtaining the results.

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